IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner:	Michelle Estrada
Serial No.:	10/623,794	Group Art Unit:	2823
Filed:	July 21, 2003	Docket:	1303.108US1
Title:	GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION		

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
10/052952	January 17, 2002	1303.034US1	THREE-DIMENSIONAL PHOTONIC CRYSTAL WAVEGUIDE STRUCTURE AND METHOD
10/382246	March 5, 2003	1303.086US1	CELLULAR MATERIALS FORMED USING SURFACE TRANSFORMATION
10/379749	March 5, 2003	1303.089US1	MICRO-MECHANICALLY STRAINED SEMICONDUCTOR FILM
10/425797	April 29, 2003	1303.093US1	LOCALIZED STRAINED SEMICONDUCTOR ON INSULATOR
10/431134	May 7, 2003	1303.094US1	STRAINED Si/SiGe STRUCTURES BY ION IMPLANTATION
10/425484	April 29, 2003	1303.095US1	STRAINED SEMICONDUCTOR BY WAFER BONDING WITH MISORIENTATION
10/443355	May 21, 2003	1303.098US1	SILICON OXYCARBIDE SUBSTRATES FOR BONDED SILICON ON INSULATOR
10/443340	May 21, 2003	1303.099US1	ULTRA-THIN SEMICONDUCTORS BONDED ON GLASS SUBSTRATES

10/431137	May 7, 2003	1303.100US1	MICROMECHANICAL STRAINED SEMICONDUCTOR BY WAFER BONDING
10/634174	August 5, 2003	1303.102US1	STRAINED Si/SiGe/SOI ISLANDS AND PROCESSES OF MAKING SAME
10/443337	May 21, 2003	1303.103US1	GETTERING OF SILICON ON INSULATOR USING RELAXED SILICON GERMANIUM EPITAXIAL PROXIMITY LAYERS
10/443339	May 21, 2003	1303.104US1	WAFER GETTERING USING RELAXED SILICON GERMANIUM EPITAXIAL PROXIMITY LAYERS
10/623788	July 21, 2003	1303.109US1	STRAINED SEMICONDUCTOR BY FULL WAFER BONDING
09/855532	May 16, 2001		METHOD OF FORMING MIRRORS BY SURFACE TRANSFORMATION OF EMPTY SPACES IN SOLID STATE MATERIALS
09/861770 6582512	May 22, 2001		METHOD OF FORMING THREE-DIMENSIONAL PHOTONIC BAND STRUCTURES IN SOLID MATERIALS
09/734547 6383924	December 13, 2000		METHOD OF FORMING BURIED CONDUCTOR PATTERNS BY SURFACE TRANSFORMATION OF EMPTY SPACES IN SOLID STATE MATERIALS
10/118350	April 9, 2002		METHOD OF FORMING SPATIAL REGIONS OF A SECOND MATERIAL IN A FIRST MATERIAL
10/093332	March 7, 2002		METHOD AND APPARATUS FOR PACKAGING SEMICONDUCTOR DEVICES
10/931554	August 31, 2004	1303.093US2	LOCALIZED STRAINED SEMICONDUCTOR ON INSULATOR

10/931749	August 31, 2004	1303.095US2	STRAINED SEMICONDUCTOR BY WAFER BONDING WITH MISORIENTATION
10/931344	August 31, 2004	1303.108US2	GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
10/931553	August 31, 2004	1303.099US2	ULTRA-THIN SEMICONDUCTORS BONDED ON GLASS SUBSTRATES
10/931580	August 31, 2004	1303.100US2	MICROMECHANICAL STRAINED SEMICONDUCTOR BY WAFER BONDING

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 10-25-04 By _____
Marvin L. Beekman
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 26 day of October, 2004.

KACIA LEE
Name

Kacia Lee
Signature